I CLAIM:

1. A clock recovery system for generating a clock signal corresponding to an asynchronous data signal, said circuit comprising:

an input port for receiving an incoming data signal;

a local oscillator circuit for generating a plurality of clock signals having the same frequency, said plurality of clock signals each being shifted in phase relative to one another;

a sampling unit having a plurality of latches, each of said latches being clocked by one of said plurality of clock signals generated by said local oscillator circuit, said sampling unit outputting a plurality data samples of said incoming data signal;

a data phase alignment unit coupled to said sampling unit, said data phase alignment unit receiving said plurality of said data samples as input signal and operative for shifting the phase of said plurality of data samples;

a multiplexer circuit coupled to said data phase alignment unit, said multiplexer circuit having a first multiplexer operative for selecting a portion of said plurality of said data samples, each of said data samples having a corresponding clock signal, which is one of said plurality of clock signals generated by said local oscillator circuit, said multiplexer circuit having a second multiplexer operative for selecting one of said plurality of clock signals generated by said local oscillator circuit;

a phase decoder coupled to said multiplexer circuit, said phase decoder operative for receiving said portion of said plurality of data samples selected by said multiplexer and for generating an output signal indicative of the logic values of the portion of said plurality of said data samples selected by said first multiplexer; and

a barrel shifter circuit coupled to said phase decoder, said barrel shifter operative for adjusting the data samples selected by said first multiplexer in accordance with the output signal of said phase decoder.

2. The clock recovery system according to claim 1, wherein said local oscillator circuit generates four clock signals having the same frequency, each of said four clock signals being out of phase with one another by 90°.

3. The clock recovery system according to claim 2, wherein said sampling unit comprises four latches, each of which comprises a d-type flip-flop, and each of which is clock by one of said four clock signals generated by said local oscillator, said sampling unit generating four data samples during one cycle of the local oscillator.

4. The clock recovery system according to claim 3, wherein said data phase alignment unit comprises a plurality of latches, each of which is a d-type flip-flop, said data phase alignment unit operative for aligning the phase of three of the four data samples generated by said sampling unit each cycle of the local oscillator.

5. The clock recovery system according to claim 4, wherein said first multiplexer selects said three data samples aligned in phase and couples said three data samples to said phase detector, said three data samples being contiguous samples, said three data samples having a middle sample which represents a recovered data signal, said second multiplexer selecting and outputting the one of said four clock signals utilized to generate said middle sample selected by said multiplexer, said output of said second multiplexer representing said recovered clock signal.

6. The clock recovery system according to claim 5, further comprising an output latch operative for receiving said middle sample selected by said first multiplexer as an input signal,

said output latch being clock by the output signal of said second multiplexer so as to synchronize said recovered data signal and said recovered clock signal.

7. The clock recovery system according to claim 1, wherein said incoming data signal is an asynchronous data signal.

8. A clock recovery system for generating a clock signal corresponding to an asynchronous data signal, said circuit comprising:

an input port for receiving an incoming data signal;

a local oscillator circuit for generating a plurality of clock signals having the same frequency, said plurality of clock signals each being shifted in phase relative to one another;

a sampling unit having a plurality of latches, each of said latches being clocked by one of said plurality of clock signals generated by said local oscillator circuit, said sampling unit outputting a plurality data samples of said incoming data signal;

a data phase alignment unit coupled to said sampling unit, said data phase alignment unit receiving said plurality of said data samples as input signal and operative for shifting the phase of said plurality of data samples;

a phase decoder unit coupled to said data phase alignment unit, said phase decoder operative for receiving plurality of data samples aligned in phase and output by said data phase alignment unit and for generating output signals indicative of the logic values of said plurality of said data samples; and

a multiplexer circuit coupled to said phase decoder unit, said multiplexer circuit having a first multiplexer operative for selecting a portion of said plurality of said output signals generated by said phase decoder, said portion of said output signals representing the logical levels of contiguous data samples, each of said data samples having a corresponding clock signal, which is

one of said plurality of clock signals generated by said local oscillator circuit, said multiplexer circuit having a second multiplexer operative for selecting one of said data samples, said multiplexer circuit having a third multiplexer operative for selecting one of said plurality of clock signals generated by said local oscillator circuit; and

a barrel shifter circuit coupled to said multiplexer, said barrel shifter operative for adjusting the portion of said plurality of output signals generated by said phase decoder selected by said first multiplexer, adjusting the one of said data samples selected by said second multiplexer, and for adjusting the one of said plurality of clock signals generated by said local oscillator circuit selected by said third multiplexer.

9. The clock recovery system according to claim 8, wherein said local oscillator circuit generates four clock signals having the same frequency, each of said four clock signals being out of phase with one another by 90°.

10. The clock recovery system according to claim 9, wherein said sampling unit comprises four latches, each of which comprises a d-type flip-flop, and each of which is clock by one of said four clock signals generated by said local oscillator, said sampling unit generating four data samples during one cycle of the local oscillator.

11. The clock recovery system according to claim 10, wherein said data phase alignment unit comprises a plurality of latches, each of which is a d-type flip-flop, said data phase alignment unit operative for aligning the phase of three of the four data samples generated by said sampling unit each cycle of the local oscillator.

12. The clock recovery system according to claim 8, wherein said incoming data signal is an asynchronous data signal.

13. A method of recovering a clock signal corresponding to a data signal, said method comprising:

receiving an incoming data signal;

generating a plurality of clock signals having the same frequency, said plurality of clock signals each being shifted in phase relative to one another;

sampling said incoming data signal by utilizing a plurality of latches, each of said latches being clocked by one of said plurality of clock signals, and outputting a plurality data samples of said incoming data signal;

aligning the phase of said plurality of data samples;

selecting a portion of said plurality of said data samples, each of said data samples having a corresponding clock signal which is one of said plurality of clock signals, said selected portion of said data samples having a middle sample which represents a recovered data signal, said clock signal corresponding to said middle sample representing said recovered clock signal;

decoding said selected portion of said plurality of said data signals so as to generate an output signal indicative of the logic values of the portion of said plurality of said selected data signals; and

adjusting the selected data samples in accordance with said output signal.

14. The method of recovering a clock signal according to claim 13, wherein four clock signals are generated, each of said four clock signals being out of phase with one another by 90°.

15. The method of recovering a clock signal according to claim 13, wherein said incoming data signal is an asynchronous data signal.

16. A clock recovery system for generating a clock signal corresponding to an asynchronous data signal, said circuit comprising:

an input port for receiving an incoming data signal;

a local oscillator circuit for generating a plurality of clock signals having the same frequency, said plurality of clock signals each being shifted in phase relative to one another;

a sampling unit having a plurality of latches, each of said latches being clocked by one of said plurality of clock signals generated by said local oscillator circuit, said sampling unit outputting a plurality data samples of said incoming data signal;

a pulse width adjustment circuit coupled to said sampling unit, said pulse width adjustment circuit operative for extending the pulse width of at least some of the data samples output by said sampling unit;

a data phase alignment unit coupled to said pulse width adjustment circuit, said data phase alignment unit receiving said plurality of said data samples as an input signal and operative for shifting the phase of said plurality of said data samples and outputting aligned data samples;

a phase decoder coupled to said data phase alignment unit, said phase decoder operative for receiving said data samples output by said data phase alignment unit and for generating a plurality of output signals each of which is indicative of the logic values of said data samples, each of said plurality of output signals of said phase decoder having a corresponding clock signal, which is one of said plurality of clock signals generated by said local oscillator circuit;

a multiplexer circuit coupled to said phase decoder, said multiplexer circuit having a first multiplexer operative for selecting one of the plurality of output signals generated by the phase decoder; a second multiplexer operative for selecting one of the data samples output by the data phase alignment unit, and a third multiplexer operative for selecting one of the clock signals generated by the local oscillator circuit; and

a barrel shifter circuit coupled to said multiplexer circuit, said barrel shifter operative for adjusting the data samples selected by said first multiplexer in accordance with the output signal of said phase decoder.

17. The clock recovery system according to claim 16, wherein said local oscillator circuit generates eight clock signals having the same frequency, each of said eight clock signals being out of phase with one another by 45°.

18. The clock recovery system according to claim 17, wherein said sampling unit comprises eight latches, each of which comprises a d-type flip-flop, and each of which is clocked by one of said eight clock signals generated by said local oscillator, said sampling unit generating eight data samples during one cycle of the local oscillator.

19. The clock recovery system according to claim 18, wherein said data phase alignment unit comprises a plurality of latches, each of which comprises a d-type flip-flop circuit, said data phase alignment unit operative for aligning the phase of three of the eight data samples associated with one of said eight clock signals and generated by said sampling unit each cycle of the local oscillator.

20. The clock recovery system according to claim 16, wherein said incoming data signal is an asynchronous data signal.

21. The clock recovery system according to claim 17, wherein said pulse width adjustment circuit operates to extend the pulse width of the incoming data signal by 3/8 of a clock cycle when said data sample received from said sampling unit is present for only 4/8 of the entire clock cycle.

22. The clock recovery system according to claim 17, wherein said pulse width adjustment circuit operates to extend the pulse width of the incoming data signal by 2/8 of a

clock cycle when said data sample received from said sampling unit is present for only 5/8 of the entire clock cycle.

23. The clock recovery system according to claim 17, wherein said pulse width adjustment circuit operates to extend the pulse width of the incoming data signal by 1/8 of a clock cycle when said data sample received from said sampling unit is present for only 6/8 of the entire clock cycle.

24. The clock recovery system according to claim 17, wherein said pulse width adjustment circuit operates not to extend the pulse width of the incoming data signal when said data sample received from said sampling unit is present for 1/8, 2/8/ 3/8 or 8/8 of the entire clock cycle.

25. A method of recovering a clock signal corresponding to a data signal, said method comprising:

receiving an incoming data signal;

generating a plurality of clock signals having the same frequency, said plurality of clock signals each being shifted in phase relative to one another;

sampling said incoming data signal by utilizing a plurality of latches, each of said latches being clocked by one of said plurality of clock signals, and outputting a plurality data samples of said incoming data signal;

adjusting the pulse width of at least some of the data samples output by said sampling unit;

aligning the phase of said plurality of data samples;

selecting a portion of said plurality of said data samples, each of said data samples having a corresponding clock signal which is one of said plurality of clock signals, said selected portion

of said data samples having a middle sample which represents a recovered data signal, said clock signal corresponding to said middle sample representing said recovered clock signal;

decoding said selected portion of said plurality of said data signals so as to generate an output signal indicative of the logic values of the portion of said plurality of said selected data signals; and

adjusting the selected data samples in accordance with said output signal.

26. The method of recovering a clock signal according to claim 25, wherein eight clock signals are generated, each of said eight clock signals being out of phase with one another by 45°.

27. The method of recovering a clock signal according to claim 25, wherein said incoming data signal is an asynchronous data signal.

28. The method of recovering a clock signal according to claim 26, wherein said pulse width of the incoming data signal is extended by 3/8 of a clock cycle when said data sample received from said sampling unit is present for only 4/8 of the entire clock cycle.

28. The method of recovering a clock signal according to claim 26, wherein said pulse width of the incoming data signal is extended by 2/8 of a clock cycle when said data sample received from said sampling unit is present for only 5/8 of the entire clock cycle.

29. The method of recovering a clock signal according to claim 26, wherein said pulse width of the incoming data signal is extended by 1/8 of a clock cycle when said data sample received from said sampling unit is present for only 6/8 of the entire clock cycle.

30. The method of recovering a clock signal according to claim 26, wherein said pulse width of the incoming data signal is not extended when said data sample received from said sampling unit is present for 1/8, 2/8/ 3/8 or 8/8 of an entire clock cycle.

31. A clock recovery system for generating a clock signal corresponding to an asynchronous data signal, said circuit comprising:

means for receiving an incoming data signal;

means for generating a plurality of clock signals having the same frequency, said plurality of clock signals each being shifted in phase relative to one another;

mean for sampling said incoming data signal by utilizing a plurality of latches, each of said latches being clocked by one of said plurality of clock signals, and outputting a plurality data samples of said incoming data signal;

mean for adjusting the pulse width of at least some of the data samples output by said sampling unit;

mean for aligning the phase of said plurality of data samples;

means for selecting a portion of said plurality of said data samples, each of said data samples having a corresponding clock signal which is one of said plurality of clock signals, said selected portion of said data samples having a middle sample which represents a recovered data signal, said clock signal corresponding to said middle sample representing said recovered clock signal;

means for decoding said selected portion of said plurality of said data signals so as to generate an output signal indicative of the logic values of the portion of said plurality of said selected data signals; and

means for adjusting the selected data samples in accordance with said output signal.

32. The clock recovery system for generating a clock signal corresponding to an asynchronous data signal according to claim 31, wherein said incoming data signal is an asynchronous data signal.

33. The clock recovery system according to claim 31, wherein said means for adjusting the pulse width of the incoming data signal operates to adjust the pulse width by 3/8 of a clock cycle when said data sample received from said sampling unit is present for only 4/8 of the entire clock cycle.

34. The clock recovery system according to claim 31, wherein said means for adjusting the pulse width of the incoming data signal operates to adjust the pulse width by 2/8 of a clock cycle when said data sample received from said sampling unit is present for only 5/8 of the entire clock cycle.

35. The clock recovery system according to claim 31, wherein said means for adjusting the pulse width of the incoming data signal operates to adjust the pulse width by 1/8 of a clock cycle when said data sample received from said sampling unit is present for only 6/8 of the entire clock cycle.

36. The clock recovery system according to claim 31, wherein said means for adjusting the pulse width of the incoming data signal does not extend the pulse width of the incoming data signal when said data sample received from said sampling unit is present for 1/8, 2/8/ 3/8 or 8/8 of the entire clock cycle.